Appl. No. 10/761,985
Examiner: Tran, Thien F, Art Unit 2811
In response to the Office Action dated April 27, 2006

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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-18 (Canceled)

Claim 19 (Currently amended): A transistor, comprising:

a source/drain region;

a buried strap out-diffusion region adjacent to one sidewall of a deep trench; and

a bended gate structure having a bended gate and a bended gate insulating layer, wherein the bended gate structure comprises ~~, comprising~~ a first portion extending along a first direction and a second portion extending along a second direction intersecting with the first direction, wherein the first portion of the bended gate is adjacent to the source/drain region and the second portion of bended gate is adjacent to the buried strap out-diffusion region.

Claim 20 (Previously presented): The transistor as claimed in claim 19, wherein the deep trench is a trench of a deep trench capacitor.

Claim 21 (Previously presented): The transistor as claimed in claim 19, wherein the bended gate is adjacent to a shallow trench isolation.

Claim 22 (Previously presented): The transistor as claimed in claim 19, further comprising a bit line contact electrically contacting the source/drain region.

Claim 23 (Previously presented): The transistor as claimed in claim 21, wherein a spacer is formed on a sidewall of the bended gate between the bit line contact and the bended gate.

Claim 24 (Currently amended): The transistor as claimed in claim 19, wherein the bended gate is L shaped in a cross section view.

Claim 25 (Currently amended):): The transistor as claimed in claim 19, ~~further comprising a bended gate oxide layer underlying the bended gate~~ wherein the bended gate insulating layer is L shaped in a cross section view.

Claim 26 (Previously presented): The transistor as claimed in claim 19, wherein the first direction and the second direction are perpendicular.

Claim 27 (Previously presented): The transistor as claimed in claim 19, wherein the source/drain region is disposed in a substrate.

Claim 28 (Previously presented): The transistor as claimed in claim 27, wherein the first direction is parallel to the substrate surface.

Claim 29 (Previously presented): The transistor as claimed in claim 19, wherein the second direction is parallel to a sidewall of the trench.

Claim 30 (Previously presented): A memory device, comprising a deep trench capacitor and a transistor controlling the deep trench capacitor, wherein the transistor is as claimed in claim 19.